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10/690,530	10/23/2003	Takayuki Kondo	117478	6381

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EXAMINER	
KIM, JOANNE H	
ART UNIT	PAPER NUMBER
2883	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,530	KONDO, TAKAYUKI	
	Examiner	Art Unit	
	Joanne H. Kim	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/23/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim11 is objected to because of the following informalities: in lines 2-3, "at least one of" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-7, 12 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent No. 6,693,736).**

4. Regarding claim 1, the '736 patent discloses an optical interconnection circuit between chips comprising: a substrate; a first micro tile element having a light emitting function provided on the substrate; a second micro tile element having a light receiving function provided on the substrate; an optical waveguide optically connecting the first micro tile element and the second micro tile element with each other, and including an optical waveguide member formed on the substrate; and an electrode provided on the substrate and eclectically connected to at least one of the first micro tile element and

the second micro tile element (column 14, lines 44-46 and 66-67; and column 15, lines 1-11).

5. Regarding claims 2-7 and 12, the '736 patent discloses that the electrode is a bonding pad which is a wiring electrode, the electrode is a bonding pad in a case of an integrated circuit chip being flip-chip mounted onto the substrate (Figs. 30B, 41-43 and 50). The '736 patent also discloses that the optical interconnection circuit further includes a bump electrically connected to at least one of terminals of the integrated circuit chip and is bonded to the electrode (column 14, lines 11-14; and Fig. 50); the integrated circuit chip includes at least a plurality of integrated circuit chips mounted onto the substrate and a signal is transmitted via at least the first micro tile element, the second micro tile element, and the optical waveguide (Figs. 41 and 42); the second micro tile element includes at least a plurality of second micro tile elements optically connected to a single of the optical waveguide (Figs. 41-43); the first micro tile element emits light which is to be a clock signal (column 15, line 39); and the optical waveguide is treated to prevent extraneous light from entering the optical waveguide (column 9, lines 3-6).

6. Regarding claims 19-20, the '736 patent discloses an electro-optical device comprising the optical interconnection circuit. Further, it is inherent that the optical interconnection circuit is a part of electronic equipment.

7. Claims 1-7, 12-13 and 19-20 are further rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent No. 6,690,845).

8. Regarding claim 1, the '845 patent discloses an optical interconnection circuit between chips comprising: a substrate; a first micro tile element having a light emitting function provided on the substrate; a second micro tile element having a light receiving function provided on the substrate; an optical waveguide optically connecting the first micro tile element and the second micro tile element with each other, and including an optical waveguide member formed on the substrate; and an electrode provided on the substrate and eclectically connected to at least one of the first micro tile element and the second micro tile element (column 36, lines 43-58; and Figs. 4-2, 6 and 33).

9. Regarding claims 2-7 and 12-13, the '845 patent discloses that the electrode is a bonding pad which is a wiring electrode, the electrode is a bonding pad in a case of an integrated circuit chip being flip-chip mounted onto the substrate (column 6, lines 4-10). The '845 patent also discloses that the optical interconnection circuit further includes a bump electrically connected to at least one of terminals of the integrated circuit chip and is bonded to the electrode (column 6, lines 11-12 and 45-48; and Figs. 1, 4-2 and 6); the integrated circuit chip includes at least a plurality of integrated circuit chips mounted onto the substrate and a signal is transmitted via at least the first micro tile element, the second micro tile element, and the optical waveguide (Figs. 6 and 21); the second micro tile element includes at least a plurality of second micro tile elements optically connected to a single of the optical waveguide (column 39, lines 5-9; and Fig. 6); the first micro tile element emits light which is to be a clock signal (column 39, lines 35-36); the optical waveguide is treated to prevent extraneous light from entering the optical waveguide (column 12, lines 9-11); and the first micro tile element includes at least a

plurality of first micro tile elements emitting light having at least two kinds of wavelengths on the substrate (column 39, lines 5-9; and column 34, lines 52-55).

10. Regarding claims 19-20, the '846 patent discloses an electro-optical device comprising the optical interconnection circuit. Further, it is inherent that the optical interconnection circuit is a part of electronic equipment.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **. Claims 8-11 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the '736 patent**

13. Regarding claim 8, the '736 patent as discussed above in paragraph 4 discloses the optical interconnection circuit comprising the first micro tile element having a light emitting function and the second micro tile element having a light receiving function, and the waveguide optically connecting the first micro tile element and the second micro tile element formed on the substrate.

The '736 patent does not explicitly disclose that the substrate is an element of a flat panel display.

It would have been obvious to one of ordinary skill in the art that the substrate is an element of a flat panel display since it was known in the art that the optical circuit

such as that taught by the '736 patent is used in optical display devices such as a flat panel display.

Additionally, the '736 patent discloses that the optical interconnection circuit includes an integrated circuit to time control and an integrated circuit to provide driving being mounted onto the substrate as the integrated circuit chip, and the optical waveguide including at least one optical waveguide which is provided between the integrated circuit to time control and the integrated circuit to provide driving (column 15, lines 12-24 and 35-40; and Fig. 42).

14. Regarding claims 9-11, the '736 patent discloses that the integrated circuit to provide driving including at least a plurality of integrated circuits are mounted onto the substrate and at least a single optical waveguide is provided for each of the integrated circuits to provide driving; the integrated circuit to time control is electrically connected to the first micro tile element which corresponds to the integrated circuit to provide driving mounted onto the substrate; and the integrated circuit to provide driving is electrically connected to at least one of the second micro tile element (column15, lines 12-39).

15. Regarding claim 13, the '736 patent discloses the optical interconnection circuit comprising the first micro tile element includes at least a plurality of first micro tile elements (column 30, lines 54-55; and Figs. 41 and 42).

The '736 patent does not explicitly disclose that the plurality of first micro tile elements emit light having at least two kinds of wavelengths to the optical waveguide.

It is well known that an array of light emitting elements, such as LD, is used to simultaneous transmit different wavelength signals in a single waveguide.

Accordingly, it would have been obvious to one of ordinary skill in the art that the plurality of first micro tile elements emit light having at least two kinds of wavelengths to the waveguide since it was known in the art.

16. Regarding claim 14, the '736 patent discloses that the optical waveguide includes a light scattering mechanism which is installed in the vicinity of one of the first micro tile element and the second micro tile element (column 34, lines 37-51; and Fig. 64).

17. Regarding claims 15-18, the '736 patent discloses that the optical waveguide includes the light scattering mechanism.

The '736 patent does not specifically discloses that the light scattering mechanism is composed of a resin mixed with a light scattering particle, a resin of which a surface includes irregularity, the optical waveguide of which at least one of the line width and the height differ from the other, or one of a dome-shaped resin and glass in which a light scattering particle is dispersed.

It is well known to use a resin mixed with a light scattering particle as a scattering means in an optical devices. Further, it is well known that irregularity of a surface causes scattering of light.

It would have been obvious to one of ordinary skill in the art to use the light scattering mechanism composed of a resin mixed with a light scattering particle, a resin in which a light scattering particle is dispersed, a resin of which a surface includes irregularity, or the optical waveguide including a surface having irregularity (i.e., at least

one of the line width and the height differ from the other) since it was known in the art. Further, it would have been obvious to one of ordinary skill in the art to use a dome-shaped resin since it would have been an obvious matter of design choice since such a modification would have involved a mere change in the shape of a component.

18. **Claims 8-11 and 14-18 are further rejected under 35 U.S.C. 103(a) as being unpatentable over the '845 patent.**

19. Regarding claim 8, the '845 patent as discussed above in paragraph 8 discloses the optical interconnection circuit comprising the first micro tile element having a light emitting function and the second micro tile element having a light receiving function, and the waveguide optically connecting the first micro tile element and the second micro tile element formed on the substrate. The '845 patent also discloses that the optical interconnection circuit includes an integrated circuit to time control and an integrated circuit to provide driving being mounted onto the substrate as the integrated circuit chip, and the optical waveguide includes at least one optical waveguide which is provided between the integrated circuit to time control and the integrated circuit to provide driving (column 39, lines 9-39).

The '736 patent does not explicitly disclose that the substrate is an element of a flat panel display.

It would have been obvious to one of ordinary skill in the art that the substrate is an element of a flat panel display since it was known in the art that the optical circuit

such as that taught by the '845 patent is used in optical display devices such as a flat panel display.

20. Regarding claims 9-11, the '845 patent discloses that the integrated circuit to provide driving includes at least a plurality of integrated circuits are mounted onto the substrate and at least a single optical waveguide is provided for each of the integrated circuits to provide driving; the integrated circuit to time control is electrically connected to the first micro tile element which corresponds to the integrated circuit to provide driving mounted onto the substrate; and the integrated circuit to provide driving is electrically connected to at least one of the second micro tile element (column 39, lines 9-39).

21. Regarding claims14-18, the '845 patent as discussed above in paragraph 8 discloses the optical interconnection circuit comprising the optical waveguide optically connecting the first micro tile element and the second micro tile element.

The '845 patent does not disclose that the optical waveguide includes a light scattering mechanism which is installed in the vicinity of one of the first micro tile element and the second micro tile element and that the light scattering mechanism is composed of a resin mixed with a light scattering particle, a resin of which a surface includes irregularity, the optical waveguide of which at least one of the line width and the height differ from the other, or one of a dome-shaped resin and glass in which a light scattering particle is dispersed.

It is well known that the optical interconnection circuit such as that taught by the '845 patent is used in optical display devices such as a flat panel display. Further, it is

well known that the known display device uses the light scattered out of a waveguide at a desired location. (See U.S. Patent No. 6,522,794)

Therefore, it would have been obvious to one of ordinary skill in the art to include a light scattering mechanism in an optical interconnection circuit since it was known in the art.

Additionally, It is well known to use a resin mixed with a light scattering particle as a scattering means in optical devices. Further, it is well known that irregularity of a surface causes scattering of the light.

Therefore, it would have been obvious to one of ordinary skill in the art to use the light scattering mechanism composed of a resin mixed with a light scattering particle, a resin in which a light scattering particle is dispersed, a resin of which a surface includes irregularity, or the optical waveguide including a surface having irregularity (i.e., at least one of the line width and the height differ from the other) since it was known in the art. Further, it would have been obvious to one of ordinary skill in the art to use a dome-shaped resin since it would have been an obvious matter of design choice since such a modification would have involved a mere change in the shape of a component.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bischel et al. (U.S. Patent No. 6,522,794) discloses a flat panel display panel comprising an optical interconnect circuit including a light emitting element, a light

receiving element, an optical waveguide optically connecting the light emitting element and the light receiving element, and an electrode eclectically connected to one of the light emitting element and the light receiving element; and

Ouchi (U.S. Patent No. 6,477,286) discloses an integrated optielectronic device for constructing electronic equipment, wherein optic and electronic devices are integrated to transmit or receive signals via optical interconnections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joanne H. Kim whose telephone number is (571) 272-2139. The examiner can normally be reached on 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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